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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,417	08/15/2003	Hung-Jen Chu	38699-8033US	1459
25096	7590	03/01/2006	EXAMINER	
PERKINS COIE LLP			NOVACEK, CHRISTY L	
PATENT-SEA			ART UNIT	
P.O. BOX 1247			2822	
SEATTLE, WA 98111-1247			PAPER NUMBER	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Advisory Action</b> <b>Before the Filing of an Appeal Brief</b>	<b>Application No.</b> 10/642,417	<b>Applicant(s)</b> CHU ET AL.	
	<b>Examiner</b> Christy L. Novacek	<b>Art Unit</b> 2822	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 08 February 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☒ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: see attached. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: \_\_\_\_\_.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: \_\_\_\_\_.  
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). \_\_\_\_\_.  
13. ☐ Other: \_\_\_\_\_.

*Advisory Action*

This office action is in response to the proposed amendment filed February 8, 2006.

*Response to Proposed Amendment*

The proposed amendment to the claims will not be entered because the amendment presents additional claims without canceling a corresponding number of finally rejected claims.

*Response to Arguments*

Applicant's arguments filed February 8, 2006 have been fully considered but they are not persuasive.

Regarding the rejection of claim 13 as being unpatentable over the admitted prior art in view of West, Applicant argues that West is allegedly non-analogous art. Both the admitted prior art and West are directed to a method of making a solid-state semiconductor device. Therefore, West is analogous art.

Also regarding the rejection of claim 13, Applicant argues, "the sacrificial composite structure of West cannot be in the scribing line on the margin of the second substrate".

As previously stated, claim 1 of West recites:

“an array of integrated circuit chips bordered by scribe streets and separated by dicing lines;  
at least two sets of substantially parallel structures **within** each of said scribe streets, each set extending along the edge of a chip on opposite sides of each said dicing line, respectively;  
each of said sets comprising:  
at least one continuous barrier wall adjacent each chip, respectively; and  
at least one sacrificial composite structure in combination therewith, **between said wall and the center of said dicing line**, said composite structure being a discontinuous barrier wall comprising metal rivets interconnecting electrically conductive layers in an alternating pattern, whereby said composite structure provide mechanical

strength to said sets and simultaneously disperses the energy associated with crack propagation.” (emphasis added)

Therefore, West discloses that the resist region(s) are located at the scribing line. And by stating that the resist region can be located anywhere between the barrier wall in the scribe street and “the center of the dicing line”, West acknowledges that the resist regions can be in the scribing line.

Further regarding the rejection of claim 13, Applicant argues that there is allegedly no motivation to combine the West reference with the admitted prior art. The admitted prior art discloses a scribing line located at the periphery of the gate electrode line on a margin of a second substrate with a color filter thereon, but does not disclose forming a resist region located at the scribing line. Like the admitted prior art, West discloses a process of forming a solid-state semiconductor device on a substrate, wherein the substrate and overlying layers are subjected to a scribing process to divide the substrate into individual integrated circuits. West teaches that the overlying layers on the substrate are prone to cracking under the strain imposed by the scribing process (col. 3, ln. 36 – col. 4, ln. 50). To prevent the cracking from destroying the circuit, West teaches that it is beneficial to deposit a resist region at the scribing line over the integrated circuitry on the substrate (col. 4, ln. 56-62). West states that these resist regions can be deposited and patterned at the same time as other metal layers in the integrated circuit (col. 7, ln. 33-35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the resist regions of West over the gate electrode line and terminal and at the scribe region of the admitted prior art because West discloses that these resist regions are beneficial when used in any type of integrated circuit that is being diced and because West teaches that these resist regions can prevent crack propagation from destroying the integrated circuit.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN  
February 23, 2006

  
Zandra V. Smith  
Supervisory Patent Examiner  
24 Feb. 2006